

(12) PATENT APPLICATION PUBLICATION

(21) Application No.202511063949 A

(19) INDIA

(22) Date of filing of Application :04/07/2025

(43) Publication Date : 18/07/2025

(54) Title of the invention : A REAL-TIME COMPILER HARDWARE EMULATOR DEVICE FOR LOW-LEVEL PROGRAMMING

(51) International classification :G06F0011360000, G06F0008410000, G06F0009300000, G11C0019280000, A61B0005020500

(86) International Application No :NA
Filing Date :NA

(87) International Publication No : NA

(61) Patent of Addition to Application Number :NA
Filing Date :NA

(62) Divisional to Application Number :NA
Filing Date :NA

(71)Name of Applicant :

1)NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY

Address of Applicant :19, Knowledge Park-II, Institutional Area, Greater Noida – 201306, Uttar Pradesh, India. -----

Name of Applicant : NA

Address of Applicant : NA

(72)Name of Inventor :

1)KAKUMANU PRABHANJAN KUMAR

Address of Applicant :Department of Information Technology, Noida Institute of Engineering & Technology, Greater Noida. Greater Noida -----

(57) Abstract :

A real-time compiler hardware emulator (100) for low-level programming includes an instruction decoder (101), microcontroller (102), memory mapper (103), register display (104), flag indicators (106), display interface (107), and host communication port (108). It enables real-time execution and visualization of machine instructions, supporting debugging, learning, and embedded interfacing via GPIOs (109). The device ensures cycle-accurate emulation with physical feedback, bridging the gap between code and hardware response for low-level developers and educators.

No. of Pages : 14 No. of Claims : 5